VLSI Implementation of Fir Filter Using Modified Multi Bit Carry Look-Ahead Adder

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Abstract:

This paper presents a novel approach in the design and optimization of Finite Impulse Response (FIR) filters through the use of a modified multi-bit Carry Look-Ahead (CLA) adder for enhanced computational efficiency, speed, and power optimization. Traditional FIR filter implementations are faced with power consumption and hardware complexity, particularly in high-speed digital signal processing systems. The novel approach integrates an approximate gate-level modified CLA in the addition process that significantly reduces the computational complexity while maintaining high accuracy. The approach offers a trade-off between precision and hardware resource utilization and can be flexibly set based on the requirement of an application. Furthermore, the proposed system employs a Booth Multiplier during the multiplication process to further enhance processing efficiency. With these advanced VLSI techniques, the FIR filter achieves significant improvement in area efficiency, power consumption, and processing speed. Through extensive simulations and FPGA-based synthesis, the efficacy of the proposed design is verified, showing improved performance over conventional implementations. The results show its feasibility for real-time applications in telecommunications, biomedical signal processing, image processing, and digital audio processing. The proposed FIR filter design is a significant contribution to low-power, high-performance VLSI-based digital signal processing.

Keywords:

VLSI design, FIR filter, Carry Look-Ahead Adder (CLA) Booth Multiplier, approximate computing, low-power design, digital signal processing (DSP), FPGA implementing, hardware optimization, real-time processing.