Design of a 16-Bit Signed Pipelined, Radix-4, Booth Multiplier Using Wallace Tree Architecture

Dunga Teja Kiran Babu
Department of Electronics and Communication Engineering, Maulana Azad National Institute of Technology (MANIT), Bhopal, Madhya Pradesh, India

Dr. D. K. Raghuvanshi
Department of Electronics and Communication Engineering, Maulana Azad National Institute of Technology (MANIT), Bhopal, Madhya Pradesh, India

Abstract

This project implements a pipelined 16-bit Signed Input, Radix-4, Booth Multiplier by leveraging two critical architectural strategies: the Wallace Tree and Pipelining techniques. The two most important parameters of a multiplier are speed and area. Booth's algorithm is a widely-used binary multiplication technique that improves upon traditional binary multiplication by reducing the number of partial products. The combination of Booth's algorithm with Wallace Tree architecture ensures faster summation of partial products, while pipelining further boosts performance by enabling parallelism and increasing throughput. The layouts of individual blocks such as the Booth Encoder, Booth Selector, Full-Adder, and the final Multiplier Circuit are illustrated in this report. This work presents theoretical foundations, architectural design, and implementation of these techniques on Cadence-Virtuoso to evaluate their effectiveness in optimizing multiplication operations for high-speed digital systems and also discusses its performance in terms of post-parasitic delay, area, and power consumption.

Keywords

Booth Encoder, Booth Selector, Partial Products, Wallace Tree Architecture, Pipelining.