Modeling and Performance Analysis of RRAM-Based in-Memory Computing Circuits Considering Electro-Thermal and Parasitic Effects

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Abstract

Non-ideal effects in resistive random-access memory (RRAM) crossbar arrays have become a critical factor limiting the computational accuracy of in-memory computing (IMC) circuits. In this paper, we propose a comprehensive circuit model that incorporates both electro-thermal effects of RRAM devices and parasitic effects of interconnects in crossbar arrays to analyze signal integrity issues in IMC systems. The electro-thermal behavior of the device is captured using a compact model of the RRAM device, which includes an equivalent thermal circuit network for the crossbar array. Additionally, the partial element equivalent circuit (PEEC) method is employed to extract the parasitic parameters of the interconnects, enhancing modeling and simulation efficiency compared to commercial software. These two modules are then electrically integrated into a unified circuit model in HSPICE platform. Finally, the proposed model is applied to the parallel computing circuit of neural networks, and the impacts of electro-thermal effects and parasitic crosstalk on circuit performance during image recognition are explored, which is helpful for performance optimization of neural computing circuits.

Keywords

Resistive random-access memory (RRAM), in-memory computing (IMC), electro-thermal effect, parasitic effect, signal integrity.