Enhancement of Power, Performance and Area in DFT Synthesis

S Baba Fareed
M.Tech VLSI Design, National Institute of Technology Kurukshetra, Haryana, India

Dr. Gaurav Verma
Assistant Professor, National Institute of Technology Kurukshetra, Haryana, India

Abstract:

The issues of controlling and monitoring internal nodes have grown more noticeable, especially in sequential circuits, because of the growing number of transistors in chips and the increasing in manufacturing defects, for this reason, we use DFT logic in the chip to detect manufacturing defects. Debugging and fault localization have become more complicated as a result. Design for Testability (DFT) provides a useful remedy by making it possible to detect faults in the circuit being tested effectively. Integrating DFT logic into a circuit significantly impacts its power, performance, and area. This paper explores various techniques to minimize test time and test data volume through scan compression. Additionally, it addresses power reduction during shift and capture operations by employing low-power gating and clock gating techniques. While incorporating DFT logic introduces area overhead, this increase can be compensated by utilizing multibit flop cells. Experimental results on circuits reveal that these methods substantially reduce simulation time and test data volume while lowering testing power consumption. The modest area overhead incurred is effectively offset using multibit cell, ensuring a balanced and efficient design.

Keywords:

Design for Testability (DFT), Internal Scan, Scan Compression, Low Power (LP) Gating, Clock Gating (CG), Multibit (MBIT) flop, Power, Performance, and Area (PPA).