Design and Analysis of Half Adder and Half Subtractor Circuits Using Quantum-dot Cellular Automata

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Abstract:
Quantum-dot Cellular Automata (QCA) is a promising nanoscale alternative to CMOS, offering high device density, high switching speed and very low power dissipation. Half adders and half subtractors are basic building blocks of arithmetic circuits, so compact QCA realisations of them are of practical interest. This paper presents QCA layouts of a half adder and a half subtractor that need no wire crossing. The half adder uses 23 cells and the half subtractor uses 22 cells, each occupying approximately 0.0186 μm². Both circuits were designed and simulated in QCADesigner and compared with previously reported designs in terms of cell count, area, latency, gate count and crossover type. The proposed circuits need far fewer cells than the earlier designs that use 77, 62, 55 and 45 cells, and they are within two and three cells, respectively, of the smallest half adder and half subtractor layouts reported in the literature.

Keywords:
Quantum-dot cellular automata, QCA, half adder, half subtractor, majority gate, QCADesigner, nanocomputing.