Design and Optimization of Ciphering NoC Router by FPGA

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Abstract:

Network on Chip (NoC) is one of the most crucial in developing networks and routers recently due to the improvement that has been made in the way of sending vast packets of data, technology, and protocol used for sending the packets between IP cores. Also, the NoC has removed the old techniques and protocols for sending packets through routers. The NoC is the most enhanced and efficient in working in parallel ways. In this paper, a 5x5 NoC is specifically designed for wearable applications. In addition, the proposed design used the SHA-3 and AES cryptographic cores based on Field Program Gate Array (FPGA) to ensure the security of data exchange. The first step in the process is to thoroughly assess the specific performance, security, and resource constraints related to wearable technology. Then, cryptographic techniques are adjusted to work with the FPGA environment to ensure the best performance. The building step uses the adaptable characteristics of FPGAs, allowing for the smooth incorporation of two ciphering cores into the NoC architecture. Iterative optimization is the outcome of extensive functional testing and evaluation of the initial prototypes. The enhanced design effectively attains a 10% reduction in logic gate use, a 5% improvement in data processing speed, and a 20% power consumption reduction. These enhancements are very appropriate for wearable technology with space and power constraints. With a traffic load of one gigabit per second, the system shows a data transmission rate of 1.05 gigabits per second, reducing the delay by 90 nanoseconds. This system offers robust security and outstanding performance.

Keywords:

5x5 mesh network, FPGA, sha-3, AES, cryptography, 5x5 Network on chip router, mobile application, hash algorithm, hash function, Keccak hash function, sponge function.