Energy-Efficient SAR-ADC Architecture for 6G -Applications

Uma Maheshwari T
School of Electronics and Communication Engineering, REVA University, Bangalore, Karnataka, India

Venkateshappa
School of Electronics and Communication Engineering, REVA University, Bangalore, Karnataka, India

Abstract:

This paper describes the design and integration of a low-power Successive Approximation register (SAR) analog-todigital converter (ADC) using Cadence. The design concept uses a core system consisting of a differential amplifier, a common source amplifier, an operational amplifier, and an R-2R digitalto-analog converter (DAC), all optimized for high performance and lowest power consumption. Everything has been carefully designed and characterized to meet the SAR ADC performance, noise reduction, digital-to-analog conversion, and resolution requirements. The integration of these subcircuits reflects their collective action, resulting in a robust and dynamic design process. The work is still in development. This work provides a comprehensive introduction to the implementation of SAR ADCs using Cadence by the sub-circuits design. Also shows the SAR-ADC having 6G applications. Currently, the sub-circuits have been designed and tested for results.

Keywords:

SAR ADC, Differential Amplifier, Common Source Amplifier, Operational Amplifier, R-2R DAC, Analog-toDigital Conversion, Cadence Design Suite, 6G applications.