Multicycle RV32IM Microprocessor for Edge Computing Applications

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Abstract

This paper explores the design of a multicycle RV32IM microprocessor for edge computing applications. Leveraging the modularity of the RISC-V architecture, the RV32IM processor is tailored to address the needs of low-power, high-performance devices in real-time computing scenarios. By implementing a multicycle approach, the processor splits instruction execution into stages, allowing for a more efficient use of resources compared to single-cycle designs. This approach results in reduced hardware complexity, improved clock speeds, and better power management. The paper presents the processor's design process, performance metrics, and its suitability for applications such as IoT devices, smart sensors, and low-cost edge computing platforms.

Keywords

RISC-V, RV32IM, Edge computing, Instruction set Architecture (ISA), Jump and Link (JAL), Jump and Link register (JALR).